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Patent Counsel
APPLIED MATERIALS, INC.
P. O. Box 450A
Santa Clara, CA 95052

EXAMINER	
PHAM, THANHHA S	

ART UNIT	PAPER NUMBER
2813	

DATE MAILED: 03/12/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/244,788	PARIKH, SUKETU A.	
	Examiner	Art Unit	
	Thanhha Pham	2813	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 November 2003*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *5-11,13,15-19 and 23-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *5-11,13,15-19 and 23-30* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This Office Action responses to Applicant's Amendment dated 09/02/2003 and 11/25/2003.

Applicant's Amendment dated 09/02/03 cites non-elected claims 33-42 are existed in the specification. Correction is needed since claims 33-42 were cancelled in Applicant's amendment dated 12/18/01.

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention

1. Claims 5-11 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

The specification of page 13 lines 1-20, while being enabling for depositing a first dielectric layer directly on the substrate and directly on the interconnect line wherein a cap or passivation layer (not shown in figure 6A-6B) being interposed between the substrate and the first dielectric layer, does not support for the claimed invention including limitation of "the first dielectric layer contacts the interconnect line" and

"anisotropically etching the first trench through the second dielectric layer, thereby forming a second trench extending through the second and third dielectric layer".

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

1. Claims 19 and 23-30 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claim 19, line 2, "first and second substrate interconnect lines" renders the claim indefinite. It is not clear what "first and second substrate interconnect lines" means.

In claim 6, line 1, it is not clear that what M stands for.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 5-6 and 11, as being best understood, are rejected under 35 U.S.C. 103(a) as being unpatentable over Inohara et al [US 5,976,972].

➢ With respect to claim 5, Inohara et al, figs 28-31 and col 1-19, discloses the claimed method of forming a structure on a substrate (41) including at least one interconnect line (42), the method comprising:

a) depositing a first dielectric layer (43, fig 28, col 12 lines 4-8) directly on the substrate (41) and directly on the interconnect line (42);

b) depositing a second dielectric layer (44, fig 28, col 13 lines 12-18 & 62-68) on the first dielectric layer, wherein the first and second dielectric layer comprise materials having dissimilar etching characteristics (the second layer 44 being selectively etched with respect to the first dielectric layer 43, see fig 28);

c) depositing a first mask layer (56, figs 28 and 38, col 13 lines 19-24 and col 14 lines 50-58) over the second dielectric layer wherein the first mask layer includes a first via pattern having a width T;

d) anisotropically etching the first via pattern through the second dielectric layer (figs 28 and 39, col 13 lines 19-24 and col 14 lines 59-65);

e) removing the first mask (fig 28);

f) depositing a third dielectric layer (45, fig 29, col 13 lines 24-29) on the second dielectric layer, wherein the second and third dielectric layers comprise materials having dissimilar etching characteristics (fig 30 shows the third dielectric layer 45 is etched while the second dielectric layer 44 is not) and wherein the first and third dielectric layers comprises materials having similar etching characteristics (fig 30 and col 13 lines 39-48 show the first dielectric layer 43 and the third dielectric layer 45 are etched by RIE);

g) depositing a second mask layer (47, fig 29, col 13 lines 24-36) on the third dielectric, wherein the second mask layer includes a trench pattern overlaying the first via pattern and having a width P such that T exceeds P a measure M;

h) anisotropically etching the trench pattern through the third dielectric layer, thereby forming (1) a first trench in the third dielectric layer and (2) a second via pattern (fig 30, col 13 lines 39-48);

i) anisotropically etching the second via pattern through the first dielectric layer, thereby forming a via hole extending to the substrate (via hole 48 reaching toward the substrate, figs 30 & 31, col 13 lines 39-53); and

j) anisotropically etching the first trench through the second dielectric layer, thereby forming a second trench extending through the second and third dielectric layers, wherein the via hole and the second trench are adapted for fabricating a dual damascene structure (fig 31, col 13 lines 39-53 and col 10 lines 10-18).

Inohara et al embodiment of figures 28-31 does not expressly teach the first dielectric layer (43) contacts the interconnect line (42) since the cap layer (54) being formed interposed between the first dielectric layer (43) and the interconnect line (42). Being different from the Inohara et al's embodiment of figures 28-31, claim 5 cites limitation of "the first dielectric layer contacts the interconnect line" which means lacking a cap layer interposed between the first dielectric layer and the interconnect line. However, the difference is unpatentable because, per In re Conrad 169 USPQ 170 (CCPA), it is obvious to omit feature of prior art when function thereof is not needed or wanted. Moreover, Inohara et al's another embodiment of figures 24-28 shows the first dielectric layer (43) contacts the interconnect line (42). Therefore, it would have been obvious for those skilled in the art, in view of Inohara et al, to form the first dielectric

layer contacting the interconnect line as being claimed for forming dual damascene structure as a desire of device is needed.

➢ With respect to claim 6, Inohara et al substantially discloses the claimed method including depositing a second mask layer (47, fig 29, col 13 lines 24-36) on the third dielectric, wherein the second mask layer includes a trench pattern overlaying the first via pattern and having a width P such that T exceeds P a measure M. Inohara et al does not expressly teach the measure M being at least 0.2 microns. However, the claimed range of the measure M is considered to involve routine optimization while has been held to be within the level of ordinary skill in the art. As noted in In re Aller 105 USPQ233, 255 (CCPA 1955), the selection of reaction parameters such as temperature and concentration would have been obvious.

> "Normally, it is to be expected that a change in temperature, or in concentration, or in both, would be an unpatentable modification. Under some circumstances, however, changes such as these may be impart patentability to a process if the particular ranges claimed produce a new and unexpected result which is different in kind and not merely degree from the results of the prior art...such ranges are termed "critical ranges and the applicant has the burden of proving such criticality... More particularly, where the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation."
>
> *See also In re Waite 77 USPQ 586 (CCPA1948); In re Scherl 70 USPQ 204 (CCPA 1946); In re Irmscher 66 USPQ 314 (CCPA 1945); In re Norman 66*

USPQ 308 (CCPA 1945); In re Swenson 56 USPQ 372 (CCPA 1942); In re Sola 25 USPQ 433 (CCPA 1935); In re Dreyfus 24 USPQ 52 (CCPA 1934).

➢ With respect to claim 11, Inohara et al (fig 32, col 13 lines 54-61) discloses simultaneously filling the second trench (46) and the via hole (48) with a conductive material whereby a dual damascene structure is formed.

3. Claims 13 and 15-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lin [US 6,093,632] in view of Inohara et al {US 5,976,972].

➢ With respect to claim 13, Lin, figs 4-8 and col 1-6, substantially discloses the claimed method of forming a structure on a substrate comprising step of:

a) forming a dielectric stack (3/4/10a, fig 4, col 5 lines 10-28) including an etch stop(10a);

b) depositing a first mask layer (11, fig 5, col 5 lines 29-34) on the etch stop layer wherein the first mask includes:

[1] a first via pattern having a width WV1 (see first opening between the first mask layer 11 being counted from left to right, fig 5),

[2] a second via pattern having a width WV2 (see the third opening between the first mask layer 11 being counted from left to right, fig 5), and

[3] a sacrificial etch pattern positioned between the first and second via patterns such that the sacrificial etch pattern has a width WS (see the second opening between the first mask layer 11 being counted from left to right, fig 5);

c) anisotropically etching the first and second via patterns through the etch stop layer thereby extending the first and second via patterns through the etch stop and

forming a sacrificial etch segment by anisotropically etching the sacrificial etch pattern through the etch stop layer (see fig 5, col 5 lines 29-34);

d) forming the first trench on the etch stop layer such that the first trench does not overlay the sacrificial etch segment and wherein the first trench has a width WT1 (see the left trench 15b that does not overlay the sacrificial etch segment in fig 7);

e) forming a second trench having a width WT2 on the etch stop layer such that:

[1] the second trench does not overlay the sacrificial etch segment,

[2] the sacrificial etch segment is positioned between the first and second trenches,

[3] the distance between the first and second trenches exceeds WS (see the right trench 15b that does not overlay the sacrificial etch segment wherein the distance between the left and right trenches 15b exceeding the sacrificial etch pattern's width in fig 7);

f) forming a first via hole (left via hole 12b, fig 7) underlying the first trench (the left trench 15b) such that the first via hole communicates with the first trench and with the first via pattern extending through etch stop layer (10b); and

g) forming a second via hole (right via hole 12b, fig 7) underlying the second trench (the right trench 15b) such that the second via hole communicates with the second trench and with the second via pattern extending through the etch stop layer (10b) wherein [1] the first trench and the first via hole, and [2] the second trench and the

second via hole areas adapted for forming a first dual damascene structure and a second dual damascene structure respectively.

Lin does not teach the first trench's width WT1 being narrower than the first via pattern's width WV1 and the second trench's width WT2 being narrower than the second via pattern's width WV2.

However, Inohara et al (figs 28-31, col 12 lines 60-67, col 13 lines 1-60 and col 19 lines 10-15) teaches that using the trench pattern (46) with a width narrower than the width of the via pattern (51) would prevent reduction in contact area between the contact plug in the via hole and the upper wiring in the trench of the dual-damascene structure, even when misalignment occurs in lithographing step of forming the dual damascene structure.

Therefore, it would have been obvious for those skilled in the art to modify the process of Lin by using the first trench width WT1 and the second trench width WT2 as being claimed, per taught by Inohara et al, to provide the dual-damascene structure with a good interconnection wherein the problem of reduction in contact area is prevented even though misalignment occurs when forming the dual damascene structure.

➢ With respect to claim 15, the claimed range distance between the first and second trenches exceeding WS by at least 0.02μ is considered to involve routine optimization which has been held obvious to those skilled in the art . The claim is prima facie obvious without showing that the claimed ranges achieve unexpected results relative to the prior art range. In re Woodruff, 16 USPQ2d 1935, 1937 (Fed. Cir. 1990). See also In re Huang, 40 USPQ2d 1685, 1688(Fed. Cir. 1996)(claimed ranges of a

result effective variable, which do not overlap the prior art ranges, are unpatentable unless they produce a new and unexpected result which is different in kind and not merely in degree from the results of the prior art). See also In re Boesch, 205 USPQ 215 (CCPA) (discovery of optimum value of result effective variable in known process is ordinarily within skill of art) and In re Aller, 105 USPQ 233 (CCPA 1955) (selection of optimum ranges within prior art general conditions is obvious).

➢ With respect to claim 16, Lin (fig 4, col 5 lines 10-27) discloses the etch stop layer comprises one or more dielectric materials selected from the group consisting of silicon oxides, silicon nitrides and silicon carbides.

➢ With respect to claim 17, Lin (fig 8, col 6 lines 9-25) discloses simultaneously filling the first and second trenches, and the first and second via holes with a conductive material (whereby first and second dual damascene structures are formed.

➢ With respect to claim 18, Lin (fig 8, col 6 lines 9-25) discloses the conductive material comprises one or more materials selected from the group consisting of metals, alloys, metallic superconductors and nonmetallic superconductors.

4. Claims 19, 23-24, and 29-30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lin [US 6,093,632] in view of Inohara e al [US 5,976,972].

➢ With respect to claim 19, Lin, figs 4-8 and col 1-6, substantially discloses the claimed method of forming a structure on a substrate wherein the substrate includes first and second interconnect line, the method comprising step of:

a) depositing a first dielectric layer (4, fig 4, col 5 lines 10-28) directly on the substrate (1) and directly on the first and second interconnect lines (2);

b) depositing a second dielectric layer (10a, fig 4) on the first dielectric layer, wherein the first and second dielectric layers comprise materials having dissimilar etching characteristics (the first dielectric layer comprising silicon oxide 4 having dissimilar etching characteristics to the second dielectric layer 10b comprising silicon nitride, the first dielectric layer being etched selectively to the second dielectric layer – see col 5 lines 56-66);

c) depositing a first mask layer (11, fig 5, col 5 lines 29-34) on the second dielectric layer wherein the first mask includes:

[1] a first via pattern having a width WV1 (see first opening between the first mask layer 11 being counted from left to right, fig 5) wherein the first via pattern overlays the first interconnect line,

[2] a second via pattern having a width WV2 (see the third opening between the first mask layer 11 being counted from left to right, fig 5) wherein the second via pattern overlays the second interconnect line, and

[3] a sacrificial etch pattern positioned between the first and second via patterns such that the sacrificial etch pattern has a width WS (see the second opening between the first mask layer 11 being counted from left to right, fig 5);

d) anisotropically etching the first and second via patterns through the second dielectric layer and forming a sacrificial etch segment by simultaneously anisotropically etching the sacrificial etch pattern through the second dielectric layer (see fig 5, col 5 lines 29-34);

e) removing the first mask layer (see fig 6, col 5 lines 43-45);

f) depositing a third dielectric layer (13, fig 6, col 5 lines 44-48) on the second dielectric layer (10b) and in the first and second via patterns that are formed in the second dielectric layer, wherein the second and third dielectric layers comprise materials having dissimilar etching characteristics (the third dielectric layer 13 comprising silicon oxide having dissimilar etching characteristics to the second dielectric layer 10b comprising silicon nitride, the third dielectric layer being etched selectively to the second dielectric layer – see col 5 lines 56-66);

g) depositing a second mask layer (14, fig 6) on the third dielectric layer (13), wherein the second mask includes:

[1] a first trench pattern overlaying the first via pattern and the third dielectric layer, and having a width WT1(see fig 6, the left trench opening 15a in the second mask 14 that overlays the first via pattern 12a and the third dielectric layer 13), and

[2] a second trench pattern having a width WT2 overlaying the second via pattern and the third dielectric layer (see fig 6, the right trench opening 15a in the second mask 14 that overlays the "second" via pattern 12a (the third opening between the first mask layer 11 being counted from left to right) and the third dielectric layer 13) , and having a distance D between the first and second trench patterns wherein D exceeds WS (see figs 6-7 for details);

h) anisotropically etching the first and second trench patterns through the third dielectric layer, thereby forming a first trench and a second trench, additionally forming a third via pattern and a fourth via pattern by etching the first and second trench

patterns respectively through the third dielectric layer material that is deposited in the first and second via patterns respectively in the second dielectric layer (see figs 6-7 and col 5 lines 54-66 wherein the third dielectric 13 deposited in the first and second via patterns 12a being etched through to form the first and second trenches 15b, the third and fourth via patterned is formed by etching the first and second trench patterns respectively through the third dielectric layer 13 that is deposited in the first and second via patterns 12a respectively in the second dielectric layer 10b); and

i) anisotropically etching the third and fourth via patterns through the first dielectric layer thereby forming the first via hole contacting the first interconnect line and the second via hole contacting the second interconnect line, wherein

[1] the first trench and the first via hole are adapted for forming a first dual damascene structure, and

[2] the second trench and the second via hole are adapted for forming a second dual-damascene

(see figs 6-7 and col 5 lines 54-66 wherein the first via hole (left opening 12b) being formed by etching the third via pattern through the first dielectric layer 4, and the second via hole (right opening 12b) being formed by etching the third via pattern through the first dielectric 4).

Lin et al does not teach the first and second trench pattern widths WT1 and WT2 respectively narrower than the first and second via pattern widths WV1 and WV2.

However, Inohara et al (figs 28-31, col 12 lines 60-67, col 13 lines 1-60 and col 19 lines 10-15) teaches that using the trench pattern (46) with a width narrower than the

width of the via pattern (51) would prevent reduction in contact area between the contact plug in the via hole and the upper wiring in the trench of the dual-damascene structure, even when misalignment occurs in lithographing step of forming the dual damascene structure.

Therefore, it would have been obvious for those skilled in the art to modify the process of Lin by using the first and second trench widths WT1 & WT2 respectively narrower than the first and second via widths WV1 & WV2 as being claimed, per taught by Inohara et al, to provide the dual-damascene structure with a good interconnection wherein the problem of reduction in contact area is prevented even though misalignment occurs when forming the dual damascene structure.

➢ With respect to claim 23, Lin (figs 6-7 and col 5 lines 23-25, 46-48 & 54-56) discloses the first and third dielectric layer comprise materials having similar etching characteristics (the first dielectric layer comprising silicon oxide 4 while the third dielectric layer comprising silicon oxide 13, the first dielectric layer and the second dielectric layer are etched by the first selective RIE).

➢ With respect to claim 24, Lin in view of Inohara et al substantially discloses the claimed method including depositing a second mask layer (14, fig 6) including a first trench pattern and a second trench pattern wherein a distance D between the first and second trench patterns exceeds the width WS of the sacrificial etch pattern (see figs 6-7 for details). Lin does expressly teach D exceeding WS by at least 0.2 μ. However, the claimed range of value of D exceeding WS is considered to involve routine optimization while has been held to be within the level of ordinary skill in the art. As

noted in In re Aller 105 USPQ233, 255 (CCPA 1955), the selection of reaction parameters such as temperature and concentration would have been obvious. See also In re Waite 77 USPQ 586 (CCPA1948); In re Scherl 70 USPQ 204 (CCPA 1946); In re Irmscher 66 USPQ 314 (CCPA 1945); In re Norman 66 USPQ 308 (CCPA 1945); In re Swenson 56 USPQ 372 (CCPA 1942); In re Sola 25 USPQ 433 (CCPA 1935); In re Dreyfus 24 USPQ 52 (CCPA 1934).

➢ With respect to claim 29, Lin (fig 8, col 6 lines 9-25) discloses simultaneously filling [1] the first trench and the first via hole, and [2] the second trench and the second via hole with a conductive material whereby first and second dual damascene structures are formed.

➢ With respect to claim 30, Lin (fig 8, col 6 lines 9-25) discloses the conductive material comprises one or more materials selected from the group consisting of metals, alloys, metallic superconductors and nonmetallic superconductors.

5. Claims 7-8 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Inohara et al [US 5,976,972] as applied to claim 5 above, in further view of Applied Materials Inc., "Applied Materials Announces Breakthrough low K dielectric film for High-Speed Cooper Chips", Business Wire, 10/6/1998, pp 1072 and Zhao et al, "A Cu/Low-k Dual Damascene Interconnect for High Performance and Low Cost Integrated Circuits", VLSI Technology 1998, Digest of Technical Paper 1998 Symposium, pp 28-29.

With respect to claims 7-8 and 10, Inohara et al substantially discloses the claimed method including using the second dielectric layer comprising one or more

materials selected from the group consisting of silicon nitrides, silicon oxides and silicon carbides. Inohara et al does not expressly teach using the first and third dielectric layers comprising Black Diamond ™, amorphous fluorinated carbon, organic spin-on material, spin-on glass, aero-gel, poly(arylene) ethers, fluorinated poly(arylene) ethers or divinyl siloxane benzocyclobutane. However, these are materials having low k dielectric constant that has been known in the art to form dual damascene structure. See Zhao et al and Applied Materials Inc.'s documents as evidences. Selection of a known material based on its suitability for its intended use supported a prima facie obviousness determination in Sinclair & Carroll Co., Inc. v. Interchemical Corp. , 325 U.S. 327, 65 USPQ 297 (1945) "Reading a list and selecting a known compound to meet known requirements is no more ingenious than selecting the last piece to put in the last opening in a jig - saw puzzle." (65 USPQ at 301.). Therefore, it would have been obvious for those skilled in the art to select known low k dielectric materials as being claimed for the first and third dielectric layers in the process of Inohara et al to form a device with better interconnection wherein the improvement in speed and cross-talk noise is provided due to interconnect capacitance reduction.

6. Claims 25-27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lin [US 6,093,632] in view of Inohara et al [US 5,976,972] as applied to claim 19 above, and in further view of Applied Materials Inc., "Applied Materials Announces Breakthrough low K dielectric film for High-Speed Cooper Chips", Business Wire, 10/6/1998, pp 1072 and Zhao et al, "A Cu/Low-k Dual Damascene

Interconnect for High Performance and Low Cost Integrated Circuits", VLSI Technology 1998, Digest of Technical Paper 1998 Symposium, pp 28-29.

With respect to claims 25-27, Lin in view of Inohara et al substantially discloses the claimed method including using the second dielectric layer comprising one or more materials selected from the group consisting of silicon nitrides, silicon oxides and silicon carbides. Lin in view of Inohara does not expressly teach using the first and third dielectric layers comprising Black Diamond ™, amorphous fluorinated carbon, organic spin-on material, spin-on glass, aero-gel, poly(arylene) ethers, fluorinated poly(arylene) ethers or divinyl siloxane benzocyclobutane. However, these are materials having low k dielectric constant that has been known in the art to form dual damascene structure. See Zhao et al and Applied Materials Inc.'s documents as evidences. Selection of a known material based on its suitability for its intended use supported a prima facie obviousness determination in Sinclair & Carroll Co., Inc. v. Interchemical Corp. , 325 U.S. 327, 65 USPQ 297 (1945) "Reading a list and selecting a known compound to meet known requirements is no more ingenious than selecting the last piece to put in the last opening in a jig - saw puzzle." (65 USPQ at 301.) Therefore, it would have been obvious for those skilled in the art to select known low k dielectric materials as being claimed for the first and third dielectric layers in the process of Lin to form a device with better interconnection wherein the improvement in speed and cross-talk noise is provided due to interconnect capacitance reduction.

7. Claims 9 and 28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Inohara et al [US 5,976,972] or Lin [US 6,093,632] in view of Inohara et al [US

5,976,972] as applied to claims 5 or 19 above, and further in view of Ellingboe et al [US 6,114,250].

Inohara et al and Lin in view of Inohara et al substantially discloses the claimed method except expressly teaching using the first mask layer of combination of photoresist mask and hard mask layer.

However, using the combination of photoresist mask and hard mask layer as the mask layer is a known technique for etching opening in dielectric layer to form dual damascene. See Ellingboe et al (col 1-2) as an evidence that shows using the combination of photoresist mask (102) and hard mask (104) as the mask to define via/trench pattern for etching dielectric layer (106) when the photoresist mask is ineffective as a masking material when etching the dielectric layer (106). Therefore, it would have been obvious for those skilled in the art to modify the process of Inohara et al or Lin in view of Inohara et al by using the combination of photoresist mask and hard mask layer as being claimed as known technique taught by Ellingboe et al to form the via in dual damascene.

Response to Arguments

8. Applicant's arguments filed 09/02/2003 have been fully considered but they are not persuasive.

Regard to Applicant's Argument on page 14-15, Applicant argues that Lin forming first and second trenches through the etch stop layer 10 not on the etch stop layer. The argument is not persuasive because Lin (figs 6-7) discloses the first and

second trenches (15b) being formed on the etch stop (10b) because the first and second trenches 15b are located on vertical sides of the etch stop (10b).

9. Applicant's arguments with respect to claims 5-11 and 19, 23-30 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

10. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL.** See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thanhha Pham whose telephone number is (571) 272-1696. The examiner can normally be reached on Monday-Thursday 8:00 AM - 7:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl Whitehead Jr., can be reached on (571) 272-1702. The fax phone number for the organization where this application or proceeding is assigned is (703) 308-3432.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

Thanhha Pham

JACK CHEN
PRIMARY EXAMINER